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10/657,331	09/08/2003	William C. Moyer	SC13074TH	1204

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/657,331	MOYER, WILLIAM C.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :12/05/06, 05/16/06, 02/09/06, 06/14/05, 03/21/05, 09/08/03.

1. Claims 1-23 are presented for examination. Applicant is reminded that the last page of 1449 sent by fax on 03/21/05 at 10:18 has been missing. However, there is another IDS sent by fax on 03/21/05 at 12:40. Applicant is suggested to confirm that whether these two copies should be the same in the next response. TD filed on 10/19/06 has been received.

2. Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the relation between the two registers. For example, are the two register physically separated or a subset of the other ?.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1,5,8,13,15 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshida (5,870,596).

4. As to claim 1,5,8,13,15, claims 1,5,8,13,15 are rejected based on one interpretation. See discussions below. Yoshida disclosed :

a) a memory for storing operands (see how the load and store transfer operand data to/from the memory stack in col.9, lines 65-67, col.10, lines 1-11);

b) a plurality of general purpose registers wherein each general purpose register holds multiple data elements (see the plurality of registers in col.9, lines 65-67, col.10, lines 1-11, see the bytes in each registers); and

c) processor circuitry for executing one or more instructions, at least one of the one or more instructions for transferring a plurality of data elements between the memory and the at least two of the plurality of general purpose registers (see any two of the registers R1,R4,R5,R6,R7,R8 in fig.33) wherein the at least one or more instructions specifies a number of register elements (see the loading of 4 bytes according to the internal code LDM1 to R1 in col.24, lines 14 –21, as to which element ,see the lower byte) to be transferred between each of the at least two of the plurality of general purpose registers and the memory (see also the 4 byte loaded into register R4 in col.24, lines 45-50).

5. As to applicant's argument regarding the specifying the number of data elements to be transferred to/ from each of the two registers, the relation of the two registers has never been reflected into the claim. Therefore, the two register could be the upper and lower portions of a single register. It could also be ***a*** compound register comprising a plurality of registers. The examiner holds that Yoshida must be able to recognize the upper portion (e.g. most significant bits) and the lower portion (e.g. least significant bits)

of the data bytes transferred into R1. Therefore, number of bytes (either fixed or variable) has to be specified for a proper order of transfer.

6. Claims 1-16 are also rejected under different interpretation.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida (5,870,596) in view of Honma (4,903,195).

8. As to claim 1,5,8,13, 10,15, Yoshida disclosed

a) a memory for storing operands (see how the load and store transfer operand data to/from the memory stack in col.9, lines 65-67, col.10, lines 1-11);

b) a plurality of general purpose registers wherein each general purpose register holds multiple data elements (see the plurality of registers in col.9, lines 65-67, col.10, lines 1-11, see the bytes in each registers); and

c) processor circuitry for executing one or more instructions, at least one of the one or more instructions for transferring a plurality of data elements between the memory and the at least two of the plurality of general purpose registers (see any

two of the registers R1,R4,R5,R6,R7,R8 in fig.33) wherein the at least one or more instructions specifies a number of register elements (see the loading of 4 bytes according to the internal code LDM1 to R1 in col.24, lines 14 –21, as to which element ,see the lower byte) to be transferred between each of the at least two of the plurality of general purpose registers and the memory (see also the 4 byte loaded into register R4 in col.24, lines 45-50).

9. Yoshida did not specifically show to specify the number of data elements as claimed. However, Honma disclosed a system for specifying number of data elopements to be retransfer (see col.2, lines 63-68, col.3, lines 1-8);

10. It would have been obvious to one of ordinary skill in the art to use Honma in Yoshida for specifying the number of data elements to be transferred as claimed because the use of Honma could provide Yoshida the ability to designate the number of data to be transferred on a given instruction, and it could be readily achieved by predefining the number of data elements to be specified of Honma into Yoshida with modified configuration parameter (e.g. the data width, and the number of bytes etc.) so specific number of data to be transferred of Honma could recognized by Yoshida, and because Yoshida also taught a loading of 4 bytes into each register by an internal instruction, LDM (see col.24, lines 14-50), therefore, number of bytes of data was recognizable, and which was a suggestion of the need for specifying the number of data to be transferred in order to enhance the flexibility of the system, and in doing so, provided a motivation.

11. As to claims 2,6, Yoshida also specified which of the register elements to load or store (see the load and store instructions LDM and STM to pop or push data bytes in col.23, lines 15-23).

12. As to claims 3, 7,9, 14, Yoshida did not explicitly show to fill the unspecified data element with a predetermined value as claimed. However, the examiner holds that filling any register including specified and unspecified data elements with a predetermined value is inherent feature of every system. For example, a bit (either specified or unspecified) in a register should be filled with either "0" or "1". The "0" and "1" is a predetermined value.

13. As to claims 4, 10, The examiner also holds that if all bits are zero the value has to be zero.

14. As to claims 11, 12, Yoshida was applicable to both contiguous and discontinuous (see the fetch data address incremented by 4 in col.24, lines 8-29).

15. As to claim 16, Yoshida also included total byte greater than the data elements to be transfer to each of the registers (se the six bytes from the memory area onto six registers in col.22, lines 64-67, col.23, lines 1-14).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Hinds et al. (6,170,001).

17. As to claims 1, 5,8, 10,13,15, Hinds taught at lest :

a) a memory for storing operands (see transfer between register bank and memory in col.2, lines 29-30);

b) a plurality of general purpose registers wherein each general purpose register holds multiple data elements (single precision and double precision) ; and processor circuitry for executing one or more instructions, at least one of the one or more instructions for transferring a plurality of data elements between the memory and the at least two of the plurality of general purpose registers (see either the RS or RD operands) wherein the at least one or more instructions specifies a number of register elements (see the number of odd number data words in col.2, ,lines 60-67, see also the data type bit used as specifying the single or double data size in col.10, lines 54-64) to be transferred between each of the at least two of the plurality of general purpose registers and the memory (see col.20, lines 11-48 for the detail of operand data elements in a bank of registers, see also the transfer of data words in a register bank to a memory in col.2, lines 21-42).

18. As to applicant's argument that since each general purpose register is claimed as holding multiple data elements, the number of data elements to be transferred between each of the at least two general purpose registers and the memory clearly indicate that the number of data elements refers to a number of data elements within a particular general purpose register, examiner would like to point out that since each general purpose register is claimed as holding multiple data elements, and since the relation between the at least two general purpose registers is not clearly recited in the claim, the number of data elements to be transferred between each of the at least two general purpose registers and the memory clearly does not necessarily indicate that the number of data elements refers to a number of data elements within a particular general purpose register (see "112" rejection set forth above in this action).

19. As to applicant's argument that Hinds did not specify a number of data elements within an instruction, Hinds clearly taught his VFPv1 supported vector for up to eight data elements in a single instruction (see col.20, lines 26-39).

20. As to claims 2,6, Hinds also specified which of the register elements to load or store (see the load and store instructions with specified register in col.7, lines 16-26).

21. As to claims 3,4 7,9, 10, 14, Hinds also filled the unspecified data element with a predetermined value (see the logic 0 stored into one of the uninitialized data slots in col.12, lines 53-67).

22. As to claims 11, 12, Hinds was applicable to both contiguous and discontinuous (see the single and pair of data slots in col.12, lines 55-67).

23. As to claim 16, Hinds also included total number (see the DH and DL) to be transferred greater than the number of data elements (see each of the DH and DL) to be transfer to each of the registers (see each entry in register 200 in fig.15).

24. As to clams 17,18, Hinds also included total number of data element (see single S) less than each of the registers (see the double s in a single register in fig.15) , any remaining data element was filed with a predetermined value (see the logic 0 stored in register 200 in col.12, lines 55-67) .

25. AS to claim 20, Hinds also included total number of data elements to be transferred (see the all data words specified in col.3, lines 45-55).

26. As to clams 21,22, examiner holds that contiguous and non-contiguous memory locations had been known in the art.

27. As to claim 23, Hinds taught his VFPv1 supported vector for up to eight data elements in a single instruction (see col.20, lines 26-39). Therefore, any number of data elements up to eight was a subset of data elements.

28.

29. Claims 1,5,8, 10,15, are rejected under 35 U.S.C. 102(b) as being anticipated by Inagami et al. (4,760,545).

30. As to claim 1,5,8,10,13, 15, Inagami disclosed :

a) a memory for storing operands (see the main memory in figs.1 and 2, col.1, lines 59-68);

b) a plurality of general purpose registers wherein each general

purpose register holds multiple data elements (see the plurality of registers vector registers); and

c) processor circuitry for executing one or more instructions, at least one of the one or more instructions for transferring a plurality of data elements between the memory and the at least two of the plurality of general purpose registers (see transfer of vector data elements in col.1, lines 59-68, see also the loading of data elements in col.2, lines 22-56, col.4, lines 11-68, see the operands in col.5, lines 1-4) wherein the at least one or more instructions specifies a number of register elements (see fig.4b , L being the number of vector elements to be transferred, see also the number specified by instruction in col.6, lines 52-68) to be transferred between each of the at least two of the plurality of general purpose registers and memory.

As to the applicant's argument that Inagami's L value did not specify a number of data elements transferred to/from each register of at least two registers as claimed, no relationship between the two registers has been reflected into the claim (see paragraph above). Nevertheless, applicant recites, for example, executing one or more instructions for specifying the number of data elements to be transferred between each of the at least two registers and memory (see claim 1, lines 5-11). Inagami taught an instruction parameter , L, to specify the number of data elements to be transferred to/from a vector register VR of at least two vector registers (e.g. see VR0 216 and VR1 217 in fig.5)

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Apperley (5,664,145) is cited for the teaching of specifying number of data elements to be transferred (see col.14, lines 40-53).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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